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**Lab 1 – Placement and Routing**

**Design**

Four-input 32-bit pipelined multiplier.



Files: pmul32\_4\_fm.globals, \*.view, \*.v, \*.sdc

1. **Chip outlining**

Initial core utilization: 0.5

Core-to-left, core-to-top, core-to-right, core-to-bottom: 5um

电脑萤幕画面

描述已自动生成

Figure.1 Layout

1. **P/G network design**

电脑萤幕画面

描述已自动生成

Figure.2 The layout of P/G rings and stripes

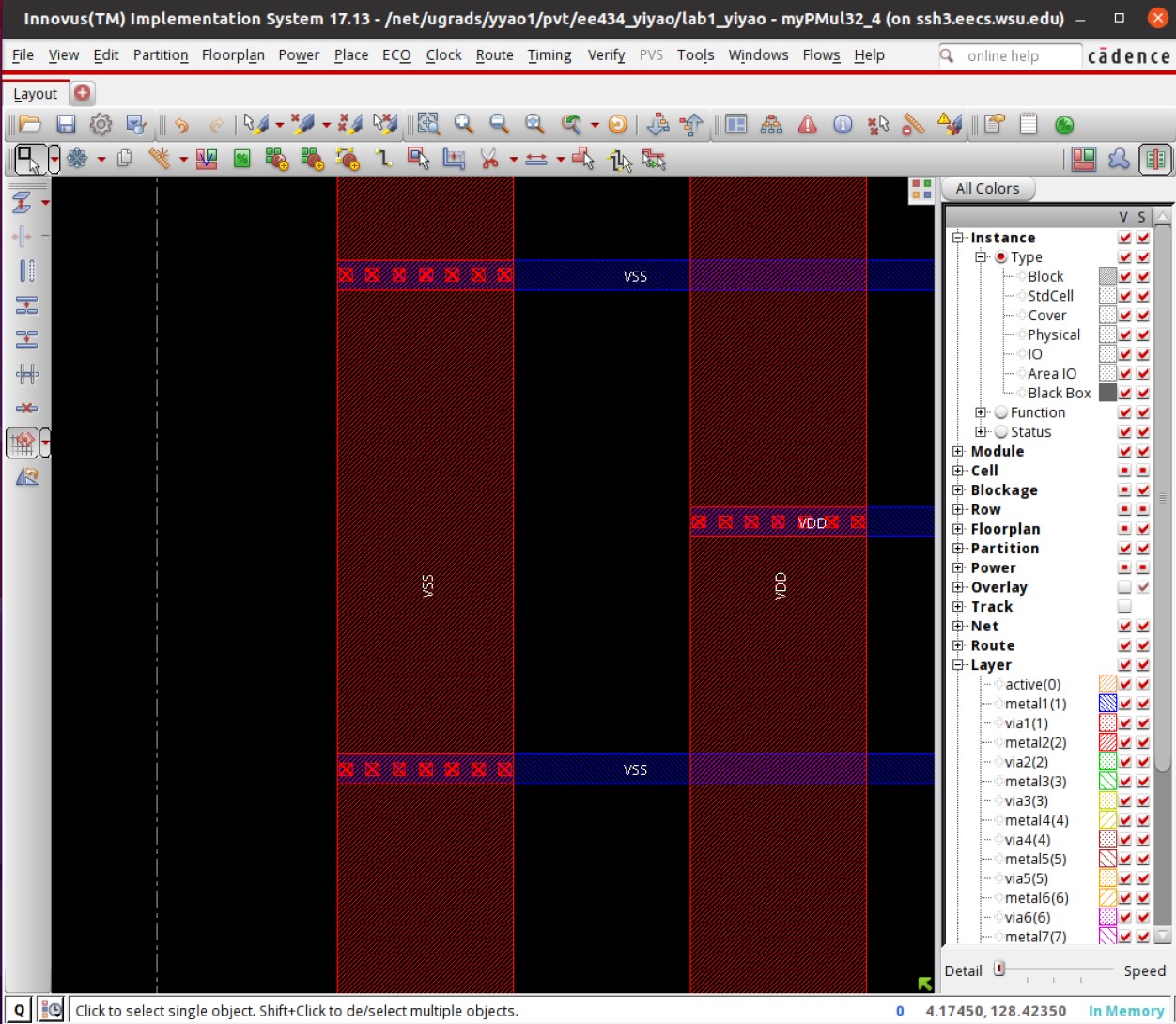


Figure.3 The detail of P/G rings and stripes

1. **Placement**

文本

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Figure.4 The layout (turn off the visibility of all the metal layers)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Placement** | **-2.171** | **-96.994** | **48.563%** | **25.8114082** | **152807.1** |

Table.1 Key values of Placement (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **Pre-CTS optimization**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Pre-CTS opt** | **0.003** | **0** | **60.631%** | **25.99783129** | **189222.8** |

Table.2 Key values of Pre-CTS optimization (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **CTS**

文本

描述已自动生成

Figure.5 The clock tree

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **CTS** | **0.001** | **0** | **60.663%** | **26.14060438** | **190232.3** |

Table.3 Key values of CTS (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **Post-CTS optimization**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Post-CTS opt** | **0.001** | **0** | **60.662%** | **26.1408024** | **190230.6** |

Table.4 Key values of Post-CTS optimization (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **Routing**

电脑萤幕画面

描述已自动生成

Figure.6 The layout of all metal layers

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Routing** | **0.02** | **0** | **60.662%** | **25.96138262** | **187590** |

Table.5 Key values of Routing (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **Post-routing optimization**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Post-Route opt** | **0.02** | **0** | **60.662%** | **25.96167634** | **187981** |

Table.6 Key values of Post-route optimization (The complete table of placement, Pre-CTS opt, CTS and etc. in the end of the report)

1. **Verification**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Cells** | **SameNet** | **Wiring** | **Antenna** |
| **Verify Geometry** | **0 Viols** | **0 Viols** | **1 Viols** | **0 Viols** |
| **Verify Connectivity** | **0 Viols** | **0 Viols** | **0 Viols** | **0 Viols** |

Table.7 Key values of Verification

**Index:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **WNS(ns)** | **TNS(ns)** | **Density(%)** | **Power(mW)** | **Wire length(um)** |
| **Placement** | **-2.171** | **-96.994** | **48.563%** | **25.8114082** | **152807.1** |
| **Pre-CTS opt** | **0.003** | **0** | **60.631%** | **25.99783129** | **189222.8** |
| **CTS** | **0.001** | **0** | **60.663%** | **26.14060438** | **190232.3** |
| **Post-CTS opt** | **0.001** | **0** | **60.662%** | **26.1408024** | **190230.6** |
| **Routing** | **0.02** | **0** | **60.662%** | **25.96138262** | **187590** |
| **Post-Route opt** | **0.02** | **0** | **60.662%** | **25.96167634** | **187981** |

Table.7 Total Key values of Chip